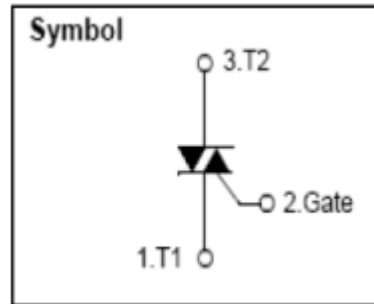


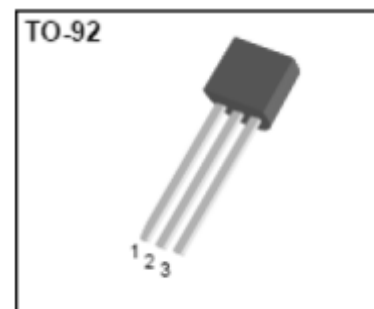
**Features**

- Repetitive Peak off-State Voltage: 800V
- R.M.S On-State Current( $I_{T(RMS)}$ )=1A
- Low on-state voltage:  $V_{TM}=1.2(\text{typ.})@ I_{TM}$
- Low reverse and forward blocking current:  
 $I_{DRM}=500\mu A@TC=125^{\circ}C$
- Low holding current:  $I_H=4mA(\text{typ.})$
- High Commutation  $dV/dt$ .



**General Description**

General purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.



**Absolute Maximum Ratings** ( $T_J=25^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DRM}$	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	800	V
$T_{(RMS)}$	Forward Current RMS (All Conduction Angles, $T_L=50^{\circ}C$ )	1	A
$I_{TSM}$	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	9.1/10	A
$I_{t}$	Circuit Fusing Considerations ( $t_p= 10\text{ ms}$ )	0.41	$A^2s$
$P_{GM}$	Peak Gate Power — Forward, ( $T_c = 58^{\circ}C$ , Pulse with $\leq 1.0\mu s$ )	5	W
$P_{G(AV)}$	Average Gate Power — Forward, (Over any 20ms period)	0.1	W
$dV/dt$	Critical rate of rise of on-state current $I_{TM} = 1.5A$ ; $I_G = 200mA$ ; $dI_G/dt = 200mA/ms$	$T_J=125^{\circ}C$ 50	$A/\mu s$
$I_{FGM}$	Peak Gate Current — Forward, $T_j = 125^{\circ}C$ (20 $\mu s$ , 120 PPS)	0.5	A
$V_{RGM}$	Peak Gate Voltage — Reverse, $T_j = 125^{\circ}C$ (20 $\mu s$ , 120 PPS)	6	V
$T_J$	Junction Temperature	-40 ~ 125	$^{\circ}C$
$T_{stg}$	Storage Temperature	-40~150	$^{\circ}C$
	mass	2	g

**Note1:** Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on-state. The rate of rise of current should not exceed 3A/ $\mu s$ .

**Thermal Characteristics**

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{QJC}$	Thermal Resistance, Junction-to-Case	-	-	60	$^{\circ}C/W$
$R_{QJA}$	Thermal Resistance, Junction-to-Ambient	-	-	120	$^{\circ}C/W$

## Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Characteristics	Min	Typ.	Max	Unit	
I <sub>DRM</sub>	V <sub>D</sub> =V <sub>DRM</sub> , Single Phase, Half Wave T <sub>J</sub> =125°C	-	-	0.5	m A	
V <sub>TM</sub>	Forward "On" Voltage (ITM = 1.5 A) (Note2)	-	1.2	1.5	V	
I <sub>GT</sub>	Gate Trigger Current (Continuous dc) (V <sub>D</sub> = 12 Vdc, R <sub>L</sub> = 33 Ω)	T2+G+	-	0.4	5	mA
		T2+G-	-	1.3	5	
		T2-G-	-	1.4	5	
		T2-G+	-	3.8	7	
V <sub>GT</sub>	Gate Trigger Voltage (Continuous dc) (V <sub>D</sub> =12 Vdc, R <sub>L</sub> = 33 Ω)	T2+G+	-	-	1.2	V
		T2+G-	-	-	1.2	
		T2-G-	-	-	1.2	
		T2-G+	-	-	1.5	
V <sub>GD</sub>	Gate threshold voltage (T <sub>J</sub> =125°C, V <sub>D</sub> =V <sub>DRM</sub> , R <sub>L</sub> =3.3KΩ)	0.2	-	-	V	
dV/dt	Critical rate of rise of commutation Voltage (V <sub>D</sub> =0.67V <sub>DRM</sub> , gate open)	10	20	-	V/μs	
I <sub>H</sub>	Holding Current (V <sub>D</sub> = 12 V, I <sub>GT</sub> = 100 mA)	-	1.3	5	mA	
I <sub>L</sub>	latching current (V <sub>D</sub> = 12 V; I <sub>GT</sub> = 100 mA)	T2+G+	-	1.2	5	mA
		T2+G-	-	4.0	8	
		T2-G-	-	1.0	5	
		T2-G+	-	2.5	8	
R <sub>d</sub>	Dynamic resistance (T <sub>J</sub> =125°C)	-	-	420	mΩ	

Note 2. Forward current applied for 1 ms maximum duration, duty cycle

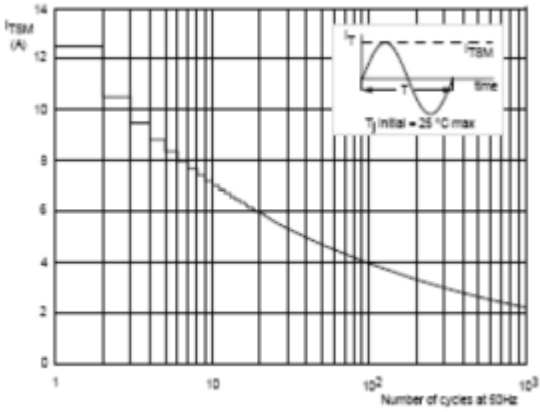


Fig.1 Maximum permissible non-repetitive Peak on-state current  $I_{TSM}$  versus number of Cycles, for sinusoidal currents,  $f=50\text{Hz}$ .

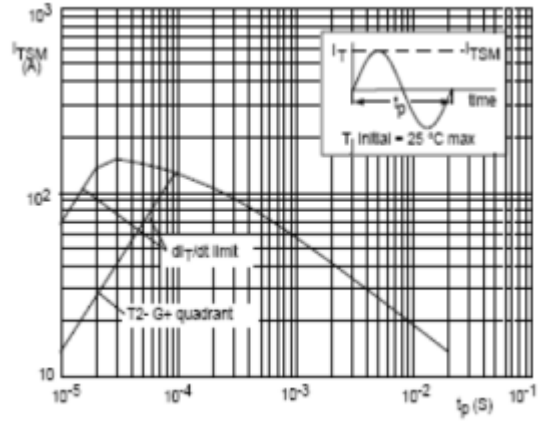


Fig.2 Maximum permissible non-repetitive Peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$  for sinusoidal currents,  $t_p \leq 20\text{ms}$

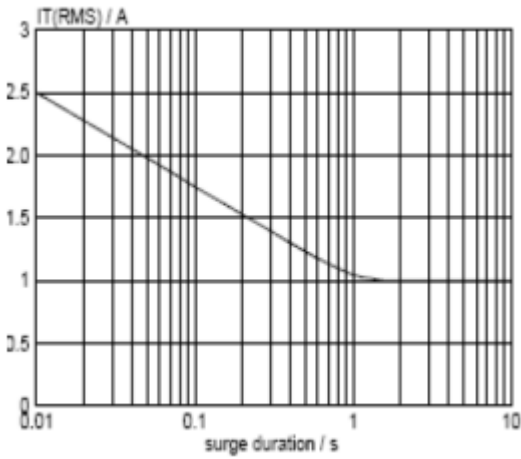


Fig.3 Maximum permissible repetitive rms On-state current  $I_{T(RMS)}$ , versus surge duration, For sinusoidal currents,  $f=50\text{Hz}$ ;  $T_{lead} \leq 66^\circ\text{C}$

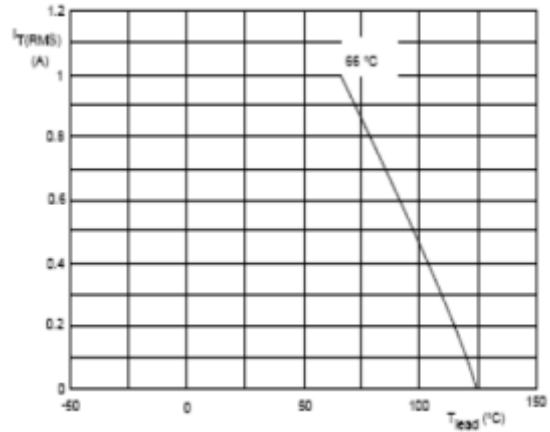


Fig.4 Maximum permissible rms current  $I_{T(RMS)}$ , versus lead temperature  $T_{lead}$

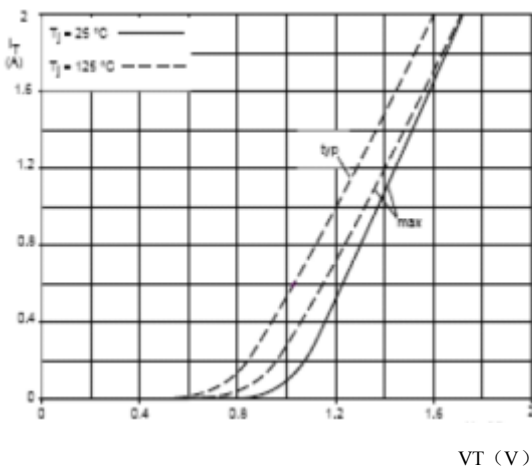


Fig.5 Typical and maximum on-state characteristic

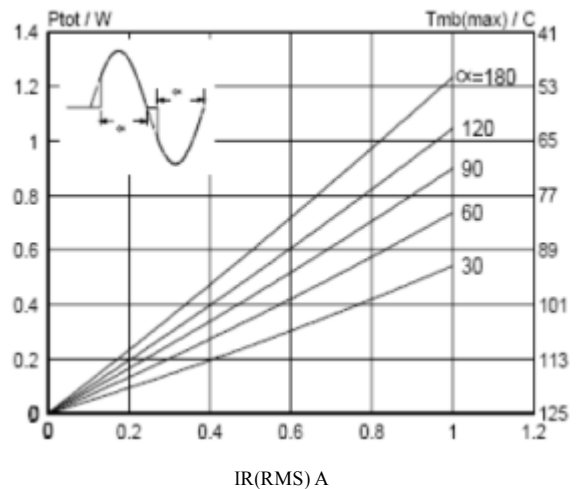


Fig.6 Maximum on-state dissipation,  $P_{tot}$  versus rms on-state current,  $I_{T(RMS)}$  where  $\alpha$ =conduction angle.

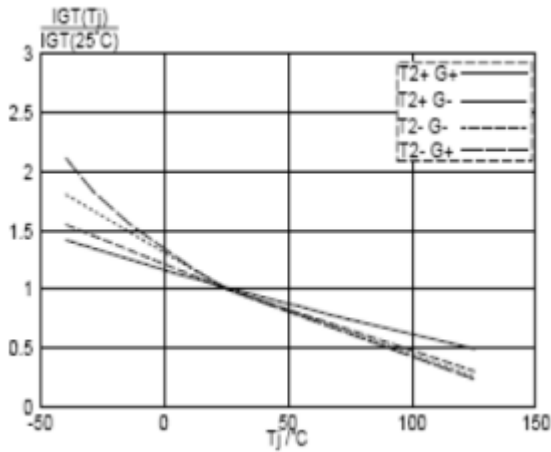


Fig.7 Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

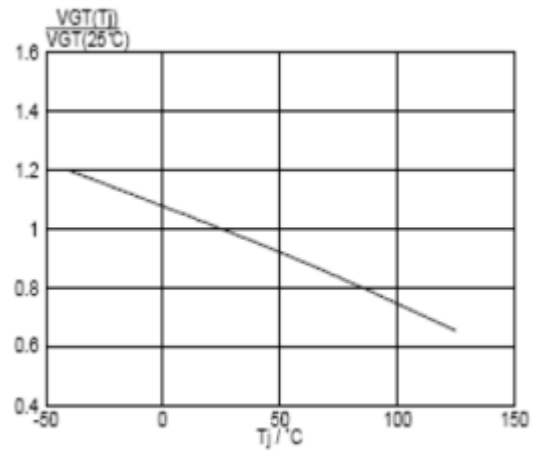


Fig.8 Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

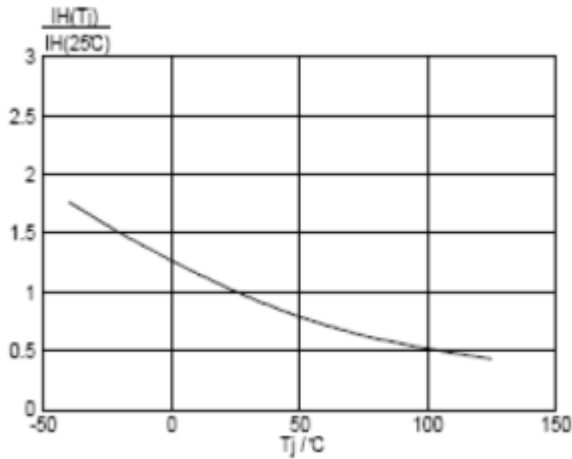


Fig.9 Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$  Versus junction temperature  $T_j$ .

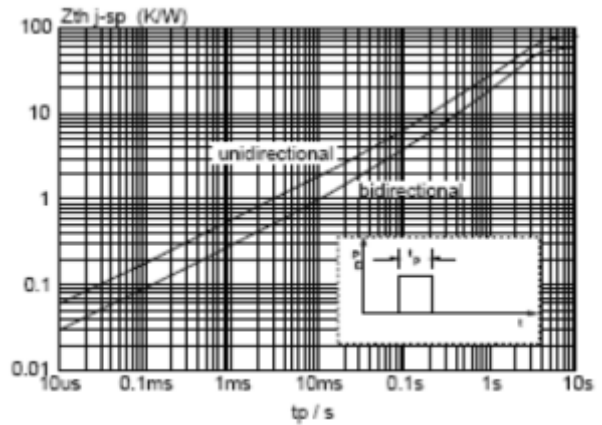


Fig.10 Transient thermal impedance  $Z_{th}$   $_{j-head}$ , versus pulse width  $t_p$ .

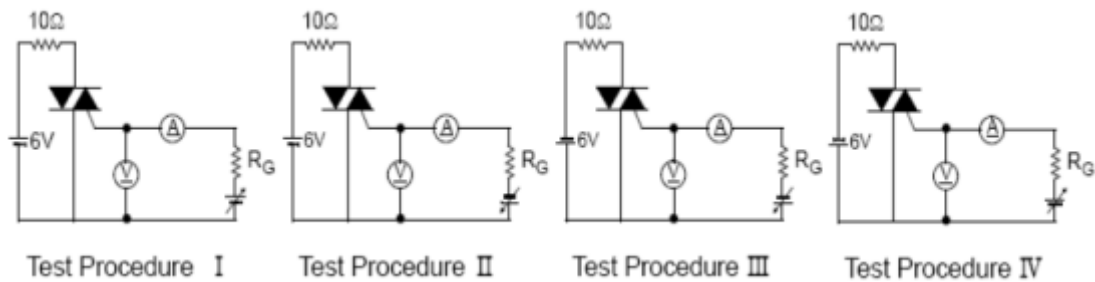


Fig.11 Gate Trigger Characteristics Test Circuit

**TO-92 Package Dimension**

