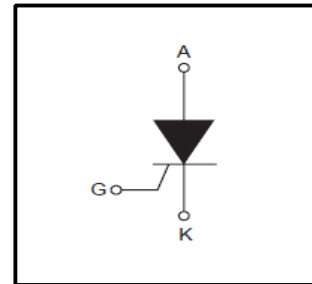


*Silicon Controlled Rectifiers*

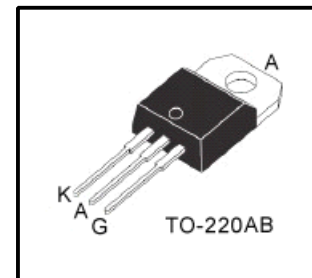
**Features**

- Sensitive gate trigger current:  $I_{GT}=200\mu A$  maximum
- Low On-State Voltage :  $V_{TM}=1.2(\text{typ.}) @ I_{TM}$
- Low reverse and forward blocking current:  
 $I_{DRM}/I_{RRM}=2mA @ TC=125^{\circ}C$
- Low holding current :  $I_H=5mA$  maximum



**General Description**

Sensitive gate triggering SCR is suitable for the application where gate current limited such as microcontrollers, logic integrated circuits, small motor control, gate driver for large SCR, sensing and detecting circuits, general purpose switching and phase control applications



**Absolute Maximum Ratings ( $T_J= 25^{\circ}C$  unless otherwise specified)**

Symbol	Parameter		Value	Units
$V_{DRM}/V_{RRM}$	Repetitive Peak Off-State Voltage (Note(1))		600	V
$I_{T(AV)}$	Average On-State Current(180° Conduction Angle)	$T_i = 110^{\circ}C$	5	A
$I_{T(RMS)}$	R.M.S On-State Current(180° Conduction Angle)	$T_i = 110^{\circ}C$	8	A
$I_{TSM}$	Non Repetitive Surge Peak on-state Current	$tp=8.3ms$	73	A
		$tp=10ms$	70	
$I^2t$	$I^2t$ Value for Fusing	$tp=10ms$	24.5	$A^2s$
$di/dt$	Critical rate of rise of on-state current $I_{TM}=2A; I_G=10mA; di_G/dt=100A/\mu s$	$T_J=125^{\circ}C$	50	$A/\mu s$
$P_{G(AV)}$	Average Gate Power Dissipation	$T_J=125^{\circ}C$	1	W
$I_{FGM}$	Peak Gate Current	$T_J=125^{\circ}C$	4	A
$V_{RGM}$	Reverse Peak Gate Voltage	$T_J=125^{\circ}C$	5	V
$T_J$	Junction Temperature		-40~125	$^{\circ}C$
$T_{STG}$	Storage Temperature		-40~150	$^{\circ}C$

**Note1:** Although not recommended, off-state Voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed  $15A/\mu s$ .

**Thermal Characteristics**

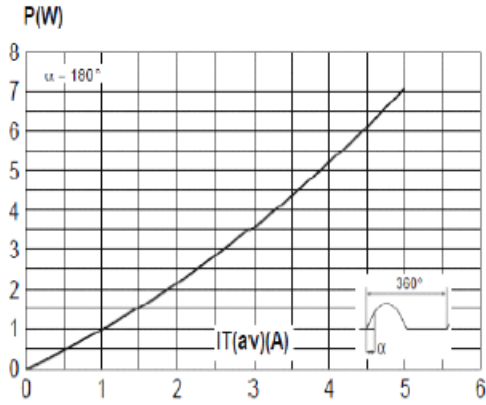
Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta Jc}$	Thermal Resistance Junction to Case	-	-	20	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	-	-	60	$^{\circ}C/W$

## Electrical Characteristics (T<sub>J</sub>=25°C ,R<sub>GK</sub>=1KΩ unless otherwise specified)

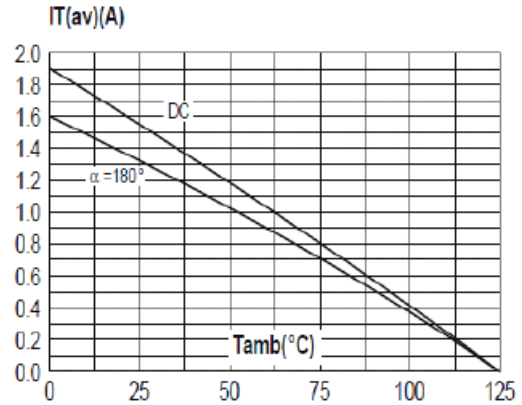
Symbol	Characteristics		Value			Units
			Min	Typ	Max	
I <sub>DRM</sub> /I <sub>RPM</sub>	Off-state leakage current (V <sub>AK</sub> =V <sub>DRM</sub> /V <sub>RPM</sub> )	T <sub>C</sub> =25°C	-	-	5	μA
		T <sub>C</sub> =125°C			1	mA
V <sub>TM</sub>	Forward "On" voltage (I <sub>TM</sub> =16A tp=380μs)  (Note2.1)		-	1.2	1.6	V
I <sub>GT</sub>	Gate Trigger Current(continuous dc) (V <sub>AK</sub> =12Vdc,R <sub>L</sub> =140Ω)  (Note2.2)		-	-	200	μA
V <sub>GT</sub>	Gate Trigger Voltage (continuous dc) (V <sub>AK</sub> =12Vdc,R <sub>L</sub> =140Ω)  (Note2.2)		-	-	0.8	V
V <sub>GD</sub>	Gate threshold Voltage (V <sub>D</sub> =12V <sub>DRM</sub> R <sub>L</sub> =3.3KΩ R <sub>GK</sub> =220Ω)  (Note2.1)		0.1	-	-	V
dv/dt	Critical Rate of Rise Off-State Voltage (V <sub>D</sub> =0.67V <sub>DRM</sub> ; R <sub>GK</sub> =220Ω)	T <sub>J</sub> =125°C	5	-	-	V/μs
I <sub>H</sub>	Holding Current(V <sub>D</sub> =12V;I <sub>GT</sub> =0.5mA)		-	2	5	mA
I <sub>L</sub>	Latching Current(V <sub>D</sub> =12V;I <sub>GT</sub> =0.5mA)		-	2	6	mA
R <sub>d</sub>	Dynamic resistance	T <sub>J</sub> =125°C	-	-	46	mΩ

**\*Notes:**

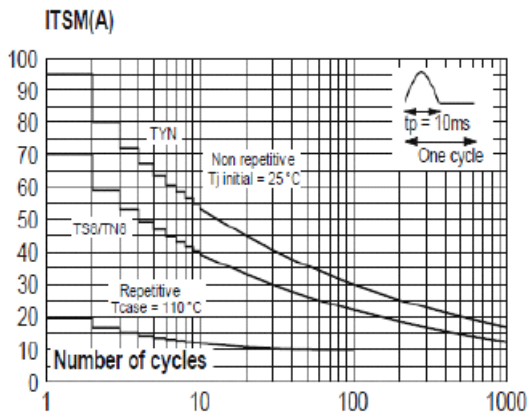
- 2.1 Pulse Width ≤1.0ms,Duty cycle≤1%
- 2.2 R<sub>GK</sub> Current is not Included in measurement.



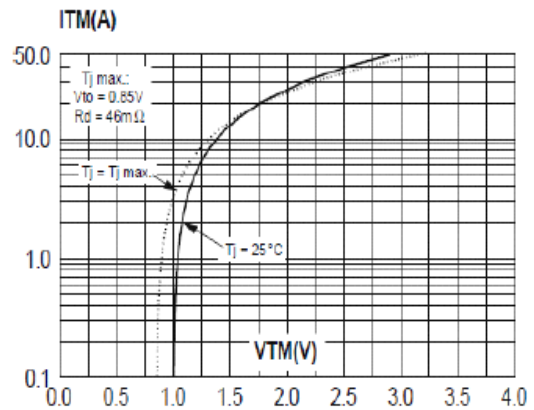
**Fig.1** Maximum average power dissipation versus average on-state current



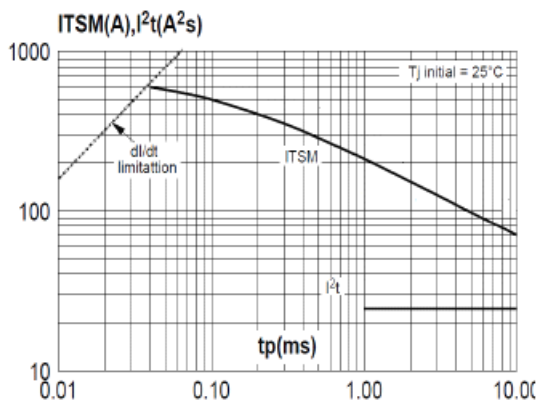
**Fig .2** Average and D.C.on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout)



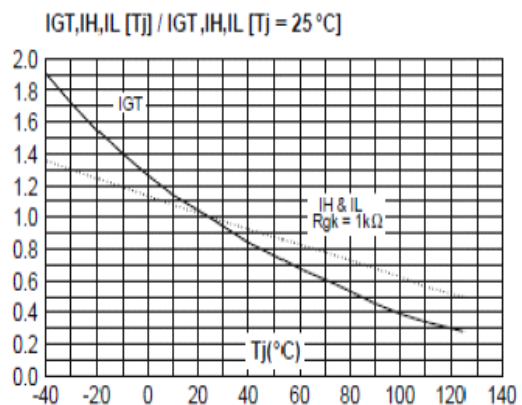
**Fig. 3** Surge peak on-state current versus Number of cycles.



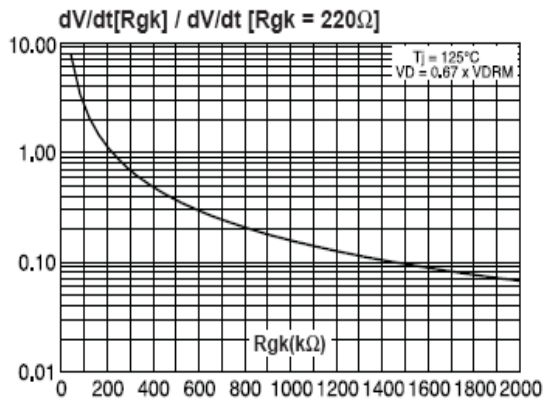
**Fig. 4** On-state Characteristics (maximum values)



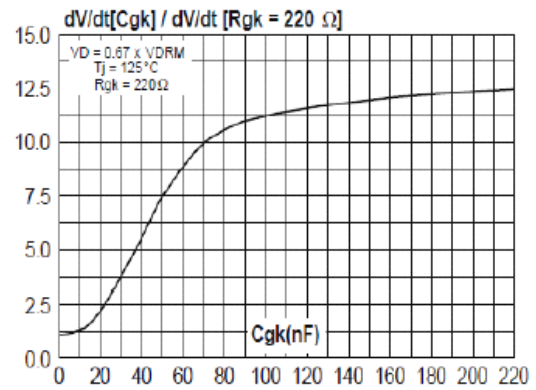
**Fig.5** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $T_p < 10ms$  and corresponding value of  $I^2t$



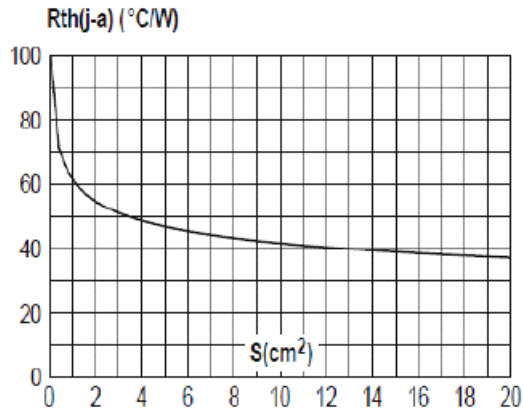
**Fig.6** Relative variation of gate trigger current and holding versus junction temperature



**Fig.7** Relative variation of dv/dt immunity versus gate-cathode resistance (typical values)



**Fig.8** Relative variation of dv/dt immunity versus gate-cathode capacitance (typical values)



**Fig.8** Thermal Resistance junction to ambient Versus copper surface under tab (Epoxy printed Circuit board FR4, copper thickness:  $35\mu\text{m}$ )

**TO-220AB Package Dimension**

